PRACTICAL M-ARY DEMODULATOR USING HARD DECISION CIRCUIT AND METHOD OF OPERATION FOR USE IN A CDMA WIRELESS NETWORK BASE STATION

ABSTRACT OF THE DISCLOSURE

A demodulator for demodulating S possible orthogonal modulation codes received serially as binary data, wherein each of the S possible orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$. The demodulator comprises Logic 00, Logic 01, Logic 10, and Logic 11 input detectors, each of which compares M/2 sequential pairs of the M binary bits of the orthogonal modulation codes to a respective one of a Logic 00 value, a Logic 01 value, a Logic 10 value, or a Logic 11 value and outputs a [+1,+1] signal if a match occurs and outputs a [-1,-1] signal if a match does not occur. An input decision circuit detects a [+1,+1] signal output by one of the input detectors after a comparison of a jth sequential pair of the M/2 sequential pairs of the M binary bits. In response to the detection, the input decision circuit adds the [+1,+1] signal to one or more of S accumulators if a jth one of the M/2 code mask bits in a corresponding one of a Logic 00 code mask, a Logic 01 code mask, a Logic 10 code mask, or a Logic 11 code mask is a Logic 1.